AMENDMENTS TO THE SPECIFICATION

Please amend the specification as follows:

On page 6, the second full paragraph:

Internal data readout circuit 3 includes a preamplifier circuit to amplify the memory cell data bits read out on global data line pairs CIO0-GIOn ~~GIOa-GIOn~~, thereby generating (n+1)-bit internal readout data.

On page 10, the third full paragraph:

In the structure of multi-bit test circuit 10 shown in Fig. 3, data bits DOUT<31:0> are supplied with the corresponding data bits in the adjacent data groups (data group IOG3 is adjacent to data group IOG0 in the cyclic manner) as teacher data. Therefore, all of readout data bits DOUT<31:0> are required to drive the input loads of ~~the~~ two EXOR circuits, which makes the driving loads on readout data bits DOUT<31:0> approximately uniform. This makes the definite timings of the input signals of EXOR circuits XR0-XR31 approximately the same, thereby making the definite timings of the output signals of EXOR circuits XR0-XR31 approximately the same. As a result, there is no need to determine the timing of taking in flag FLAG from OR circuit OGA with the variations in signal propagation delay time taken into consideration, making it possible for a next stage circuit to take in flag FLAG at a faster timing. This facilitates the timing designing for the next-stage circuit (not shown) to take in flag FLAG from OR circuit OGA.